ABSTRACT OF THE INVENTION

Disclosed is a method of aligning a mask with a semiconductor wafer surface, comprising the steps of providing a semiconductor surface with one or more wafer alignment marks thereon, providing a mask with one or more etchings effective in generating one or more 0-π-phase-conflict alignment marks under ambient lighting conditions of use, wherein each said wafer alignment mark is of a geometry that is compatibly aligning with a corresponding 0-π-phase-conflict alignment mark, and aligning said 0-π-phase-conflict alignment marks with their corresponding wafer alignment marks.